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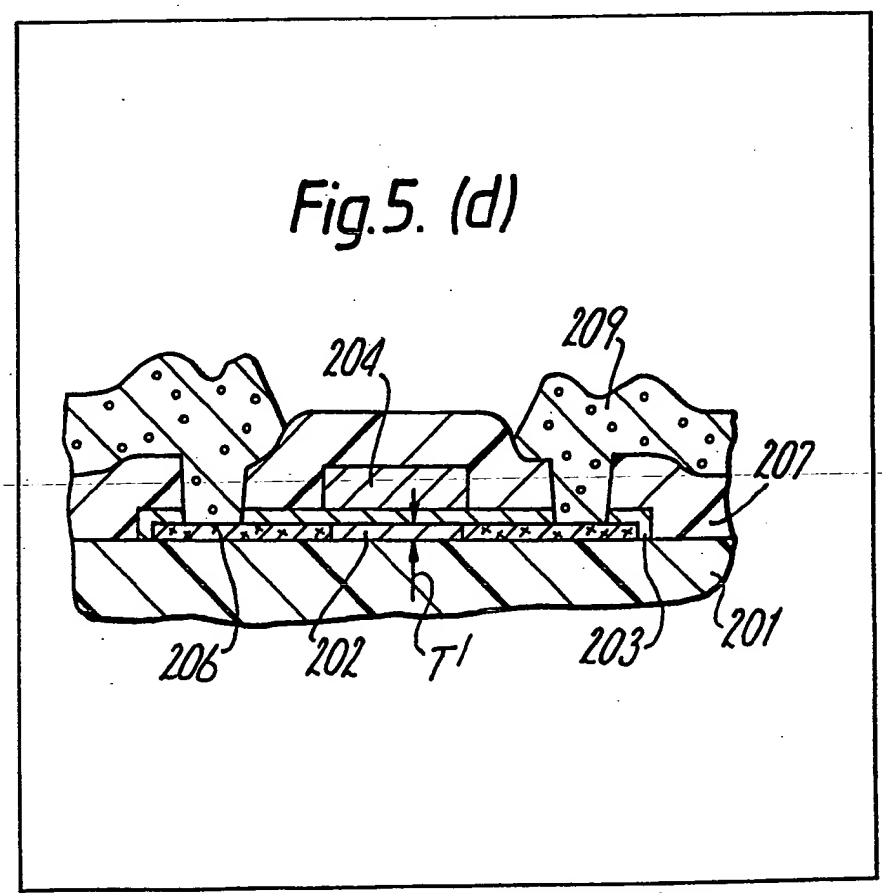
(54) **A thin film MOS transistor and an active matrix liquid crystal display device**

(57) A thin film MOS transistor includes a silicon layer (202) whose thickness, at least in the channel region is less than 2500Å. The silicon layer may be a polycrystalline silicon layer and its thickness in the channel region may be less than its thickness in the source and drain regions. Such thin film MOS transistors may be used in active matrix liquid crystal display devices having a plurality of picture elements arranged in a matrix, each picture element having a thin film MOS transistor as a switching element.



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The drawings originally filed were informal and th print here reproduced is taken from a later filed formal copy.

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Fig.1.

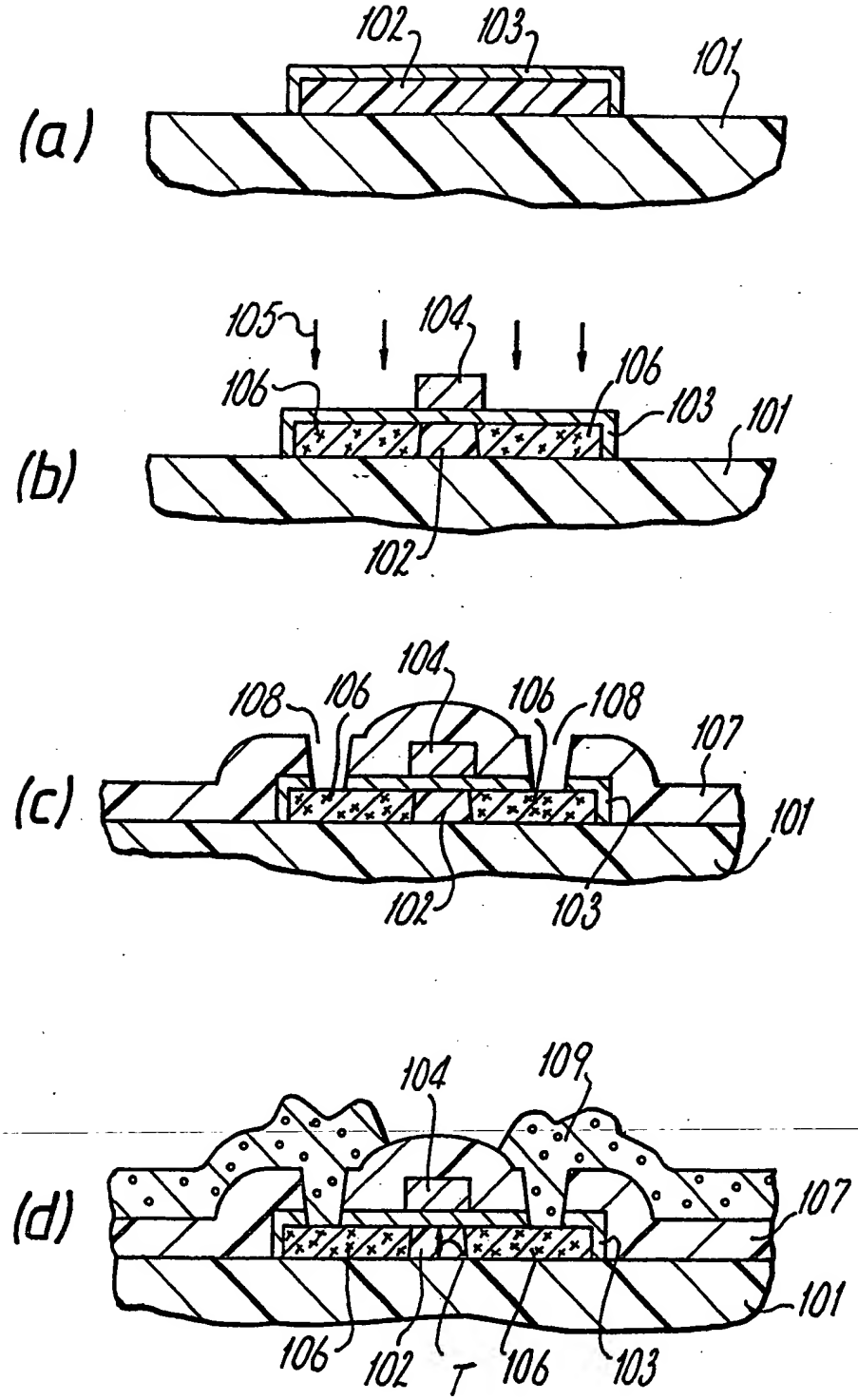


Fig.2.

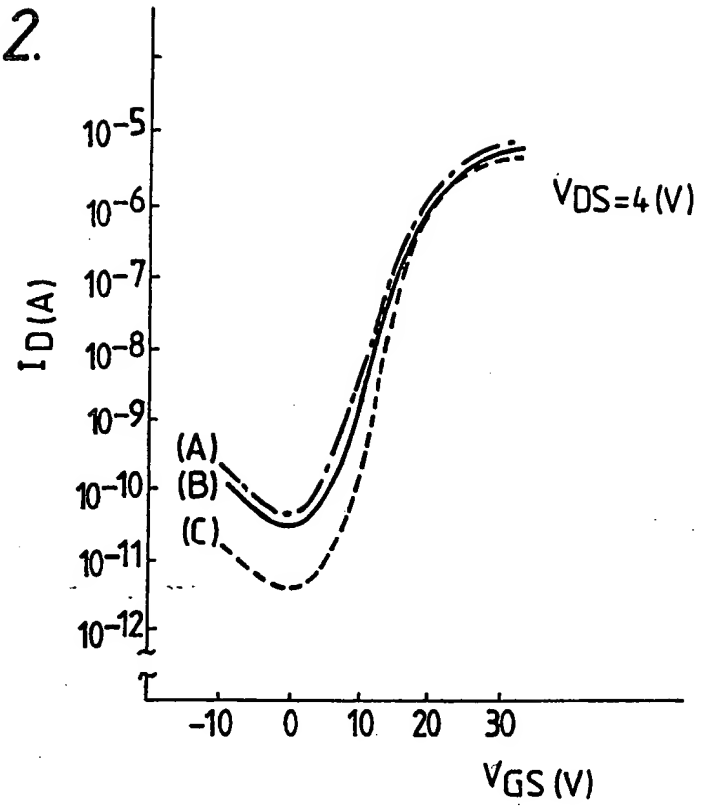

10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I_D(A)
(A)
(B)
(C)
V_{DS}=4 (V)
-10
0
10
20
30
V_{GS} (V)

Fig.3.

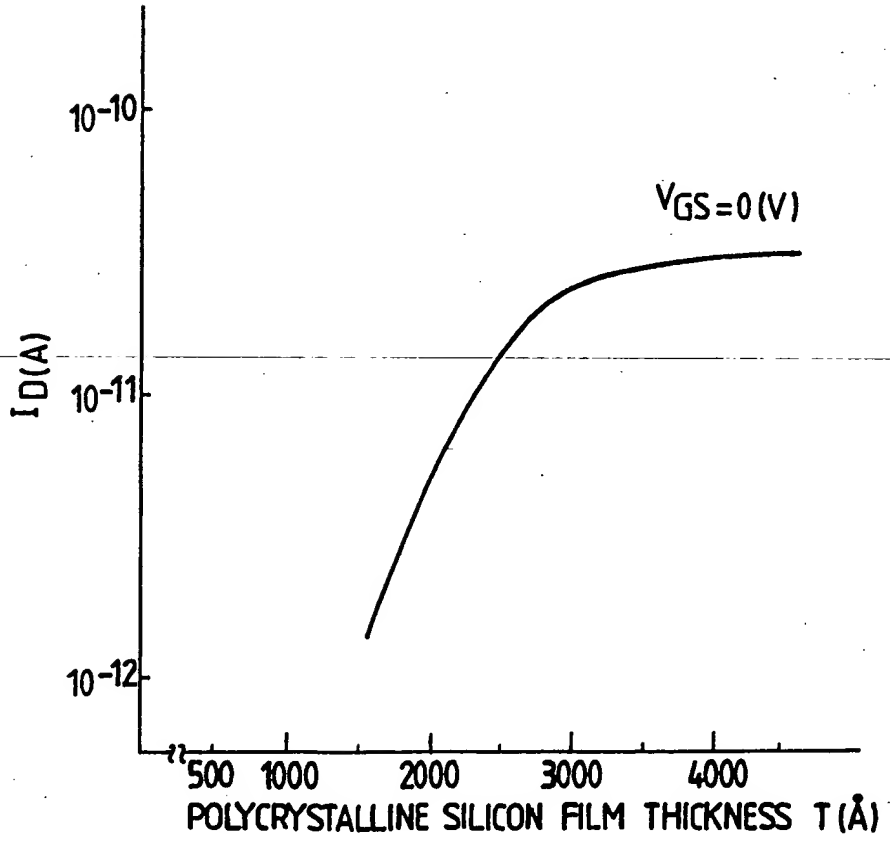
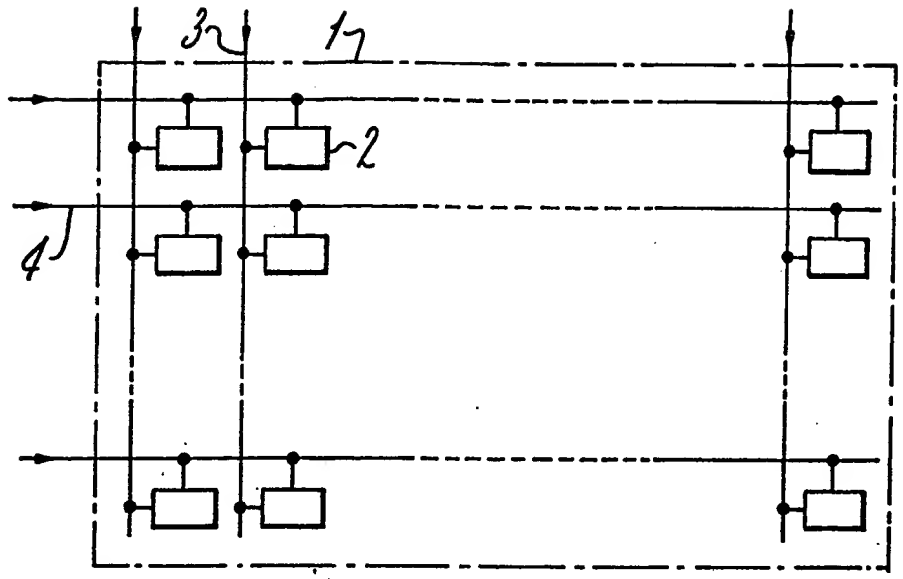

10^{-10}
10^{-11}
10^{-12}
I_D(A)
V_{GS}=0 (V)
500
1000
2000
3000
4000
POLYCRYSTALLINE SILICON FILM THICKNESS T (Å)

Fig.4.



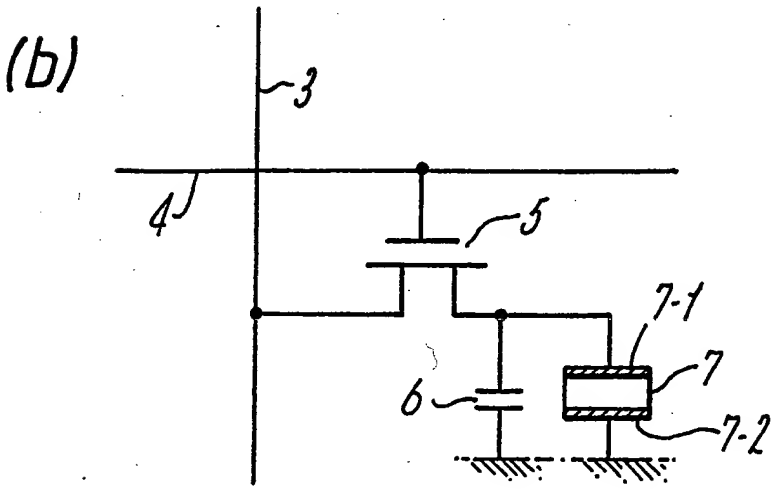


Fig.7.

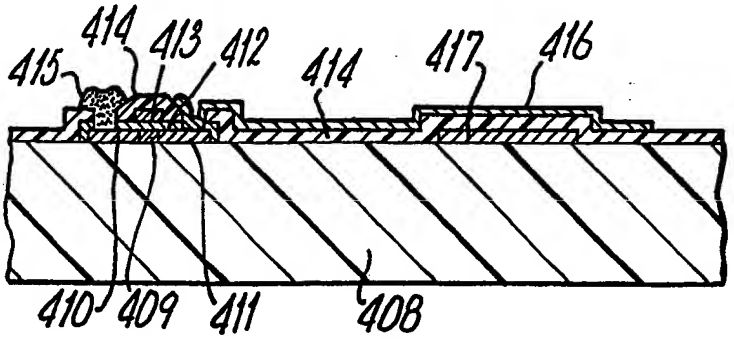
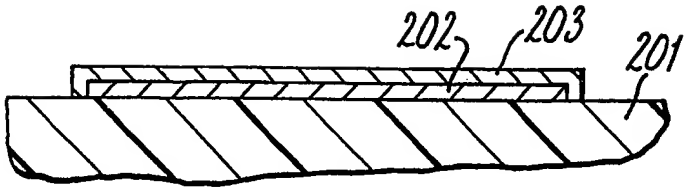
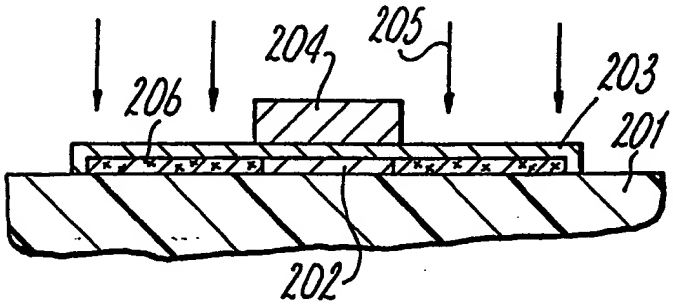


Fig.5.

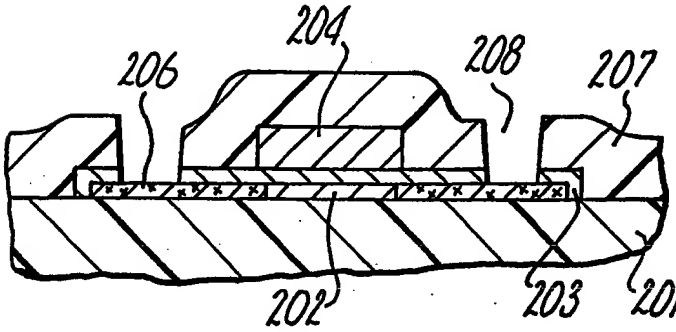
(a)


202
203
201

(b)


204
205
206
203
201
202

(c)


204
206
208
207
202
203
201

(d)

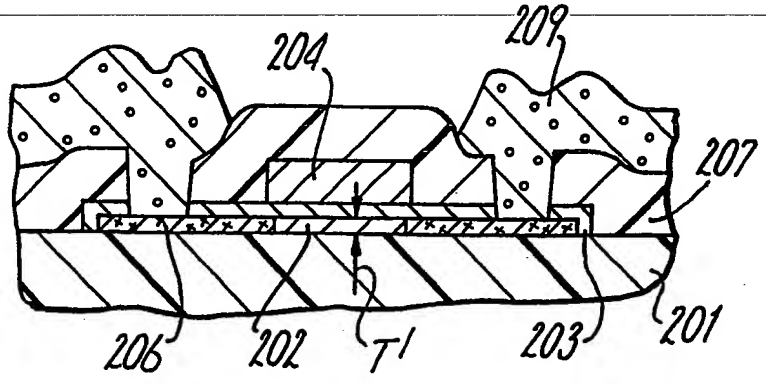

209
204
207
206
202
T1
203
201

Fig.6.

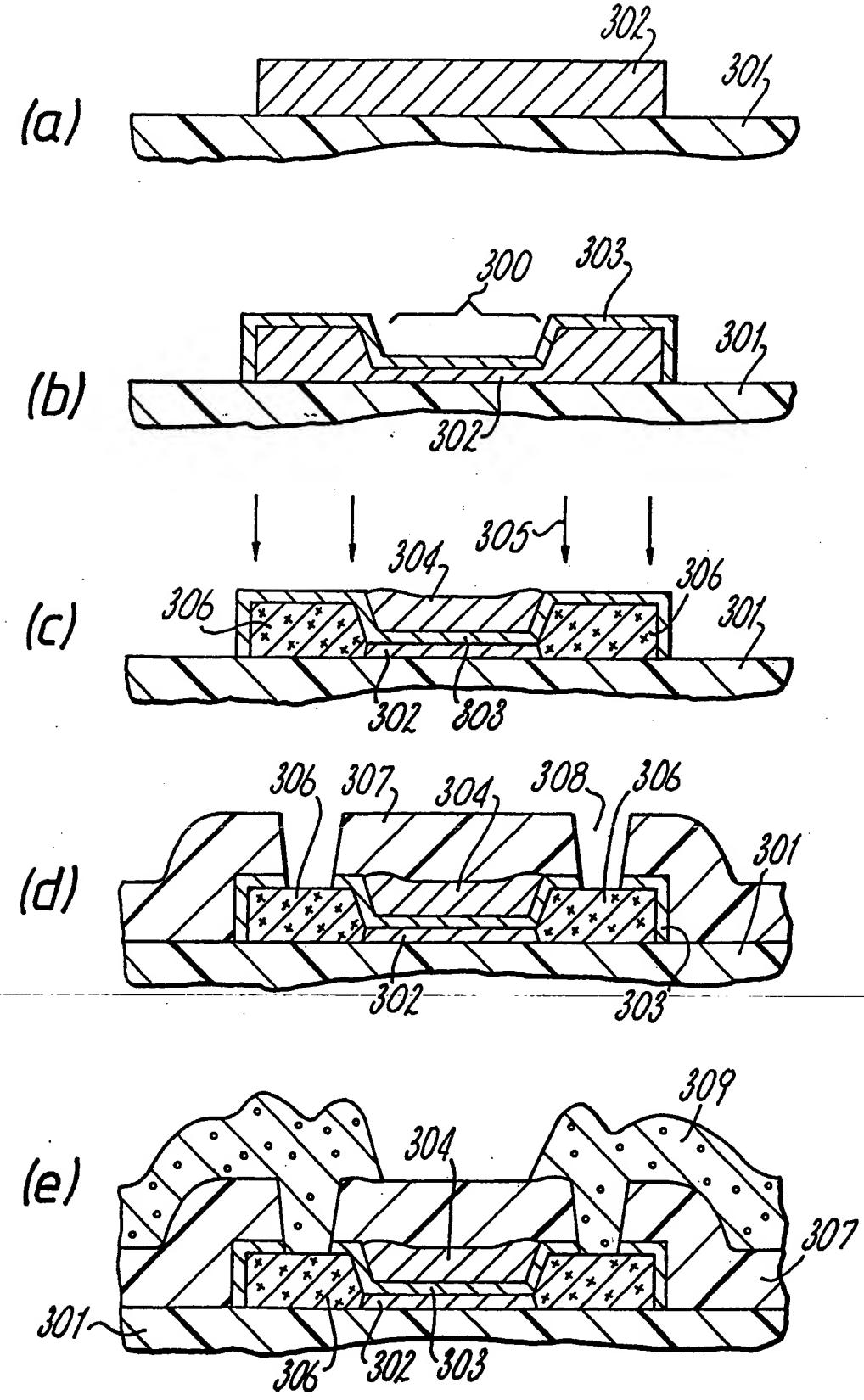

(a)
302
301
(b)
300
303
301
302
(c)
305
304
306
306
301
302
303
(d)
306
307
304
308
306
301
302
303
(e)
309
304
307
301
306
302
303

Fig.8.

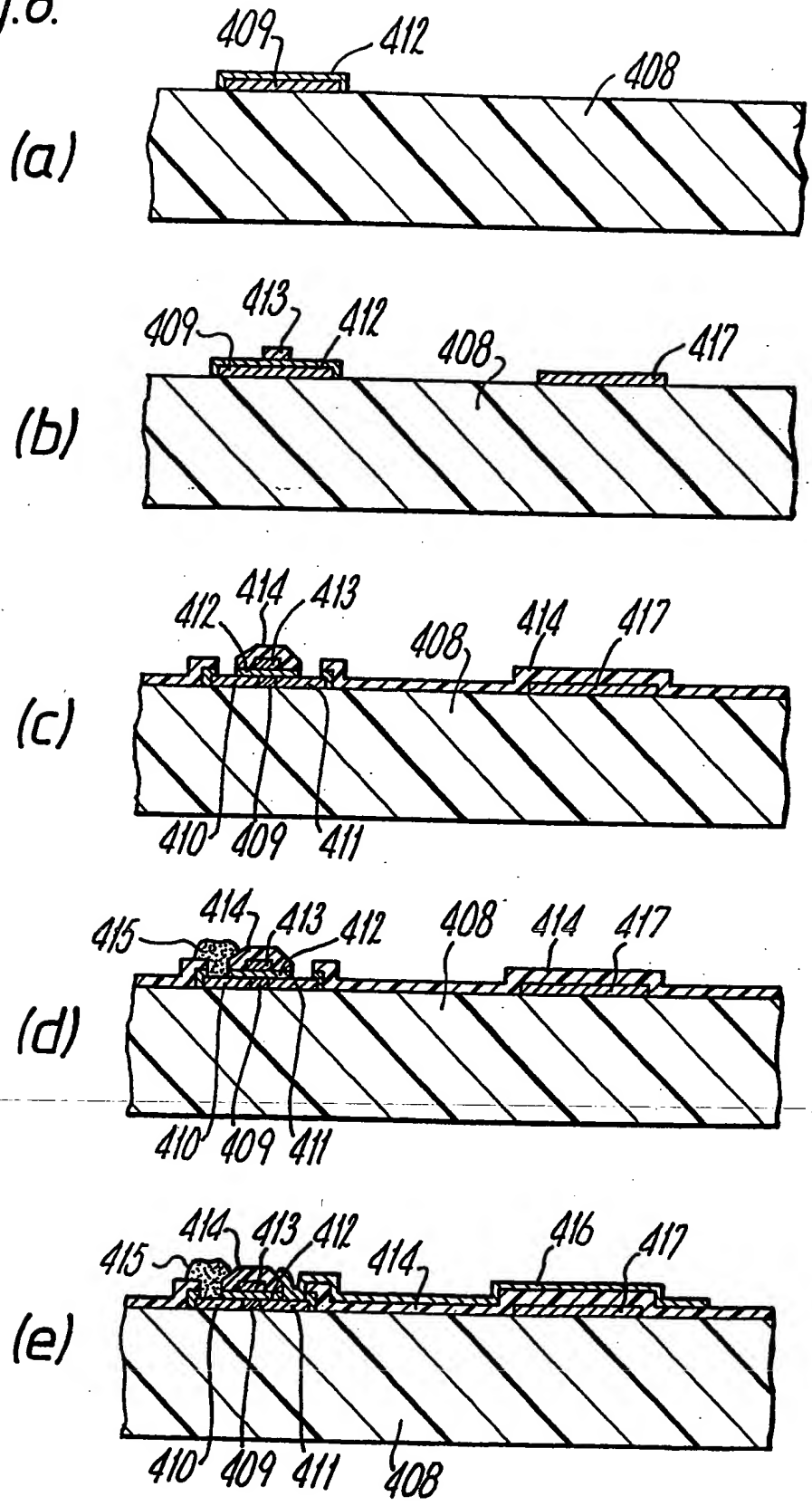

(a)
409
412
408
(b)
409
413
412
408
417
(c)
412
414
413
408
414
417
410
409
411
(d)
415
414
413
412
408
414
417
410
409
411
(e)
415
414
413
412
414
416
417
410
409
411
408

Fig.9.

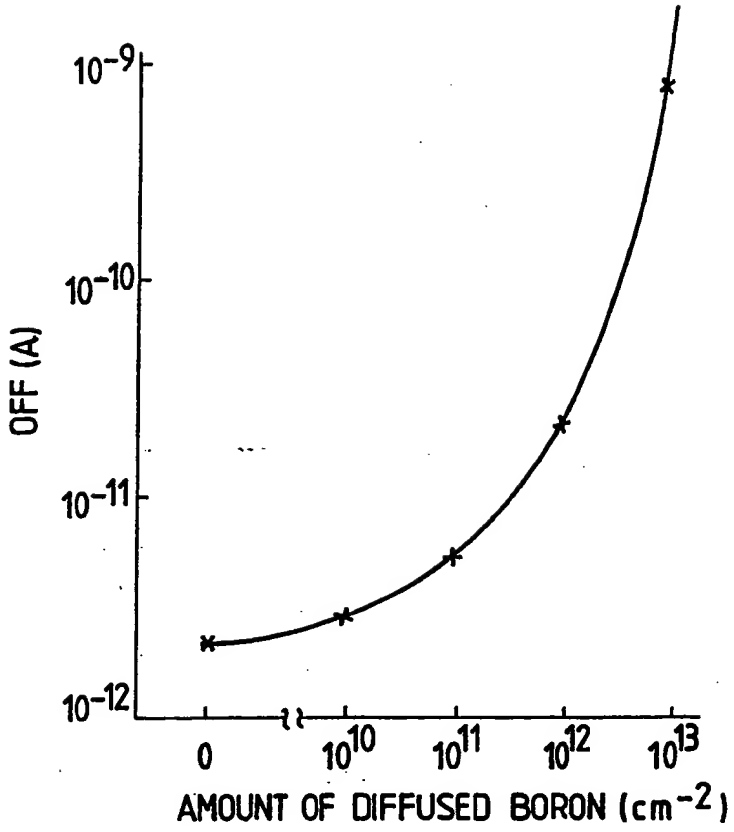
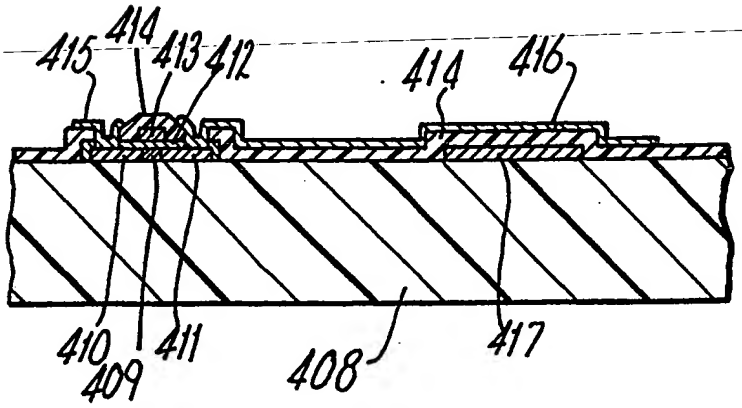

10^{-9}
10^{-10}
10^{-11}
10^{-12}
OFF (A)
0
10^{10}
10^{11}
10^{12}
10^{13}
AMOUNT OF DIFFUSED BORON (cm^{-2})

Fig.10.


415
414
413
412
414
416
410
409
411
408
417

SPECIFICATION

A thin film MOS transistor and an active matrix liquid crystal display device

This invention relates to thin film MOS transistors, for example, using a polycrystalline silicon layer or amorphous silicon layer and to active matrix liquid crystal display devices.

Recently the technology for forming thin film transistors has advanced. There are many applications of thin film transistors, for example, to active matrix liquid crystal display devices employing relatively inexpensive substrates, three-dimensional integrated circuits where active elements such as thin film transistors are formed on conventional semi-conductor integrated circuits etc. The present invention seeks to improve substantially the characteristics of thin film transistors and can be applied to other devices apart from those mentioned above.

According to one aspect of the present invention there is provided a thin film MOS transistor including a silicon layer whose thickness, at least in the channel region is less than 2500 Å.

Preferably the thickness of the silicon layer in the channel region is less than its thickness in the source and drain regions.

The silicon layer may be a polycrystalline silicon layer.

The silicon layer may be an intrinsic polycrystalline silicon layer.

According to another aspect of the present invention there is provided an active matrix liquid crystal display device having a plurality of picture elements arranged in a matrix, each picture element having a thin film MOS transistor according to the present invention as a switching element.

According to another aspect of the present invention there is provided an active matrix liquid crystal display device having a plurality of data lines and address lines arranged in columns and rows, a thin film MOS transistor and a liquid crystal driving electrode being formed at the intersection of each data line with each address line, each thin film MOS transistor having a channel region of intrinsic polycrystalline silicon.

Preferably the active matrix liquid crystal display device includes a gate insulating film formed by thermally oxidising the intrinsic polycrystalline silicon.

The data lines and the address lines may be formed from the same transparent conductive film.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 consisting of Figures 1(a) to 1(d), illustrates the steps of manufacturing a thin film transistor;

Figure 2 shows graphically the relationship between gate voltage and drain current of the thin film transistor of Figure 1;

Figure 3 shows graphically the relationship between the thickness of the polycrystallin silicon layer f the thin film transistor of Figure 1 and drain current;

Figure 4 consisting of Figures 4(a) and 4(b), illustrate the general construction of an active matrix liquid crystal display device;

Figure 5 consisting of Figures 5(a) to 5(b), illustrates the steps of manufacturing one embodiment of a thin film transistor according to the present invention;

Figure 6 consisting of Figures 6(a) and 6(e), illustrates the steps of manufacturing another embodiment of a thin film transistor according to the present invention;

Figure 7 is a cross-section of part of one embodiment of an active matrix liquid crystal display device according to the present invention;

Figure 8 consisting of Figures 8(a) to 8(e), illustrates the steps of manufacturing the liquid crystal display device of Figure 7;

Figure 9 shows graphically the relationship between concentration of impurity diffused into the channel region of an end channel thin film transistor and OFF current;

Figure 10 is a cross-section of part of another embodiment of an active matrix liquid crystal display device according to the present invention.

Figure 1 illustrates the steps of manufacturing a MOS thin film transistor. In Figure 1(a), a first thin layer of polycrystalline silicon is formed on an insulating substrate 101 and is patterned to provide an island 102. A gate insulating film 103 is formed by thermal oxidation of the island 102 or by a chemical vapour deposition technique. Subsequently, a second thin layer of polycrystalline silicon, metal silicofluoride, or metal is deposited and patterned to provide a gate electrod 104. Ion implanted impurity 105 such as phosphorus, arsenic or boron are diffused into the island 102, using the gate electrode 104 as a mask, to form source and drain regions 106 of the thin film transistor, as shown in Figure 1(b). An insulating layer 107 with contact windows 108 is then formed as shown in Figure 1(c). Finally, connector metal of, for example, aluminium, is formed as shown in Figure 1(d).

Figures 2 and 3 show graphically the characteristics of the thin film transistor manufactured as illustrated in Figure 1. In Figure 2, the abscissa represents gate voltage VGS and the ordinate represents drain current ID. The voltage VDS between drain and source regions is set at 4V. The curves (A), (B), (C) in Figure 2 show the variation of gate voltage with drain current as the thickness T of the polycrystalline silicon layer is varied. In curve (A) the thickness T is 4000Å, in curve (B) the thickness T is 3000Å and in curve (C) the thickness T is 2000Å.

Figure 3 shows a relationship between the thickness T of the polycrystalline silicon layer and the drain current ID in the case where the gate voltage VGS is zero.

From Figures 2 and 3 it will be appreciated that the leakage current of the thin film transistor in the OFF state depends on the thickness T of the polycrystalline silicon layer. The thinner the polycrystalline silicon layer the smaller the leakage current. Furthermore, it can be appreciated from Figure 3 that the leakage current ID (VGS = 0) is substantially constant when th thickness of th polycrystalline silicon layer is greater than 2500Å and sharply

decreases when it is less than 2500Å. This tendency is found to be th same in the case of other thin silicon layers, for xampl , amorphous silicon layers.

Therefore, in th manufacture of a thin film transistor, the thickness of the polycrystalline silicon layer must be controlled to an appropriate value in order to minimise leakage current in the OFF state of the thin film transistor especially in the case where the thin film transistor is used as a switching element.

An active matrix liquid crystal display device employing polycrystalline silicon thin film transistors according to the present invention as switching elements will now be described. The active matrix liquid crystal display device comprises a matrix of picture elements each 0.01 mm^2 to 0.09 mm^2, the resistance of the liquid crystal material being about 10^{10} Ω. Thus the leakage current of the thin film transistor of each picture element needs to be less than 1/10th that of the liquid crystal material at equivalent resistance, that is, less than 10^{-11}A. It has been found from experiment that the thickness T of the polycrystalline silicon layer of the thin film transistor must be less than 2500Å in order to maintain the leakage current under 10^{-11}A. An active matrix liquid crystal display device utilising thin film transistors according to the present invention as switching elements is generally composed of an upper glass substrate, a lower substrate on which the thin film transistors are formed and liquid crystal material encapsulated therebetween. Liquid crystal driving elements are formed and arranged in a matrix on one of the substrates and the picture elements are selectively energised by an external selecting circuit. Driving voltages are then applied to electrodes above the driving elements. Thus, any desired character, graphic pattern or image can be displayed by the liquid crystal display device. Figure 4 illustrates the general construction on an active matrix liquid crystal display device employing thin film transistors according to the present invention.

Figure 4(a) shows a display region 1 surrounding a plurality of liquid crystal driving elements 2 arranged in a matrix. Data signal lines 3 and timing signal lines 4 are connected to the liquid crystal driving elements 2. Figure 4(b) shows in detail one of the liquid crystal driving elements 2. A thin film transistor 5 controls the input of the data signal to a liquid crystal driving electrode 7-1. A capacitor 6 is used for holding or storing the data signal. A liquid crystal cell 7 is composed of the liquid crystal driving electrode 7-1 and an electrode 7-2 mounted on the upper glass substrate.

Thus the thin film transistor 5 is used as a switching element which selects the data signal to be applied to the liquid crystal cell in dependence upon the timing signal. Th performance of an active matrix liquid crystal display device is greatly dependent on the characteristics of the thin film transistors employed. Each of the thin film transistors 5 must, therefore, have th following characteristics:

(1) Sufficient current should flow into the capacitor 6 when the thin film transistor is in the ON state to charge it.

(2) A minimum of current should flow through the thin film transistor when it is in the OFF state.

(3) The thin film transistor must be stable, have reproducible performance and have long term reliability.

The first characteristic relates to the requirement of storing the data signal in the capacitor. The thin film transistor must accept a large flow of current so as to store the data signal completely in the capacitor in a relatively short time, since the quality of the display produced by the active matrix liquid crystal display device depends on the capacitance of the capacitor. This current flow (hereinafter referred to as "ON current") is determined by the capacitance of the capacitor and the time for writing the data signal into the capacitor. The ON current largely depends on the size (especially channel length and width), construction, manufacturing process and gate voltage of the thin film transistor. A thin film transistor with a polycrystalline silicon layer is capable of carrying sufficient ON current, and attaining the first characteristic since polycrystalline silicon has a large carrier mobility compared to that of amorphous semiconductor material.

The second characteristic relates to the holding time of the data signal written into the capacitor. Generally, the data signal written into the capacitor must be stored for a time which is long compared to the time taken to write the data signal into the capacitor. During the OFF state of the thin film transistor, the driving voltage applied to the liquid crystal driving electrode must be close to that of the data signal and so there must be little leakage current (hereinafter referred to as "OFF current") through the thin film transistor, since the capacitance of the capacitor is generally very small, for example, 1pF. If, the written data signal cannot be stored properly in the capacitor during the OFF state of the thin film transistor, then a satisfactory display will not be produced by the active matrix liquid crystal display device.

In the case where polycrystalline silicon is used in the construction of a thin film transistor there are many trap levels unevenly distributed in the crystal grains so that a relatively large leakage current can flow *via* these trap levels.

The third characteristic relates to stability, reproducibility and reliability of the characteristics of the thin film transistor. Generally, several tens of thousands of thin film transistors are formed on a substrate of an active matrix liquid crystal display device and they must have uniform characteristics and superior reproducibility with no dispersion among manufacturing batches. Moreover the thin film transistors must have long term stable reliability.

As mentioned above, a thin film transistor having a polycrystallin silicon layer has an unacceptable OFF current so that the capacitor is not capable of storing the data signal for a sufficient time during the OFF state even th ugh an acceptably large ON current can flow. Therefore, it is desirable to reduce the leakage current as much as possible. This requirement is generally desired in many applications not just active matrix liquid crystal display

devices using thin film transistors. For example, in the case of constructing a logic circuit using thin film transistors, stationary current increases and in the case of constructing a memory circuit using thin film transistors, malfunctions occur.

Conventionally, when forming the thin film transistors as active elements on a substrate, a compound semiconductor material such as cadmium-selenium or non-crystalline semiconductor material such as amorphous silicon have been used to form a thin film of semiconductor material. However, these semiconductor materials do not have all the above characteristics. For example, a compound semiconductor material has the first characteristic because of the high value of carrier mobility but not the second and third characteristics since this type of semiconductor material shows poor stability and reproducibility. Non-crystalline semiconductor material has a small carrier mobility and hence a relatively small ON current.

Figure 5 shows the steps of manufacturing one embodiment of a thin film transistor according to the present invention. The steps are similar to those described in relation to Figure 1 and so will not be explained further. The reference numerals used in Figure 5 are the same as those used in Figure 1 but increased by 100.

The thin film transistor shown in Figure 5(d) has a polycrystalline silicon layer 202 with a thickness T' which is less than 2500Å. Thus, as described above, with a thickness of this order the OFF current is minimised whereby the required performance for a device constructed using the thin film transistors is achieved.

As mentioned above, OFF current can be reduced by decreasing the thickness T' of the polycrystalline silicon layer 202, however, if it is too thin the connector metal 209 which may be aluminium or aluminium-silicon breaks through the diffusion layer, so that sufficient contact with the source and drain regions is impossible. Consequently, the control of the thickness of the polycrystalline silicon layer for decreasing OFF current is limited because the connector metal must make a stable contact with the source and drain regions, even though there is the possibility of further reducing the OFF current. To solve this problem the thickness of the polycrystalline silicon layer only in the channel region should be reduced, whereby the connector metal can be precisely in contact with the source and drain regions and yet OFF current can be reduced to the maximum extent.

Figure 6 illustrates the steps of manufacturing another embodiment of thin film transistor according to the present invention. A polycrystalline silicon layer with sufficient thickness so that subsequently connector metal can be precisely in contact with source and drain regions, is patterned to provide an island 302 as shown in Figure 6(a). The thickness of the island 302 in the channel region is reduced to be less than 2500Å by etching, thus a concave portion 300 is formed, and a gate insulating film 303 is formed by thermal oxidation or a chemical vapour deposition technique is shown in Figure 6(b). Subsequently, a second thin layer of polycrystalline silicon, metal silicofluoride or metal is deposited at the concave portion 300 and patterned to provide a gate electrode 304. Ion implanted impurities 305, such as phosphorus, arsenic or boron, are diffused into the island 302 using the gate electrode 304 as a mask so forming source and drain regions 306 as shown in Figure 6(c). Next, as shown in Figure 6(d), an insulating film 307 with contact windows 308 is formed. Finally, connector metal 309 of, for example, aluminium is formed to contact the source and drain regions 306 as shown in Figure 6(e). Thus the connector metal can be perfectly in contact with the source and drain regions whilst leakage current during the OFF state is reduced to a minimum since the thickness of the polycrystalline silicon layer in the channel region is less than 2500Å.

Figure 7 is a cross-sectional part of one embodiment of an active matrix liquid crystal display device according to the present invention. In order to simplify the drawing, only one liquid crystal driving element is shown although there are, in fact, a plurality of liquid crystal driving elements in a matrix. Thus the liquid crystal display device has a plurality of data lines and address lines arranged in columns and rows and thin film MOS transistors and a liquid crystal driving electrode formed at the intersection of each data line with each address line. A thin layer of polycrystalline silicon is deposited on an insulating substrate 408 of, for example, quartz, for forming a thin film transistor and an electrode of a capacitor. In the thin film transistor, a channel region is an intrinsic polycrystalline silicon layer 409. A source region 410 and a drain 411 are formed by doping impurity such as phosphorus, arsenic or boron into the intrinsic polycrystalline silicon layer. An address signal line is connected to a gate electrode 413 of the film thin film transistor and an insulating layer 414 functions as the dielectric of the capacitor. A data signal line 415 is connected to the source region 410 and a drive electrode 416 is connected to the drain region 411 and a common electrode 417 of the capacitor.

Figure 8 illustrates the steps of manufacturing the liquid crystal display device of Figure 7. The intrinsic polycrystalline silicon layer 409 is formed on the insulating substrate 408, and then the gate insulating film 412 is formed by thermal oxidation as shown in Figure 8(a). Then the gate electrode 413 and the common electrode 417 of the capacitor, which can be formed of the same conductive material at the same time, are formed as shown in Figure 8(b). Subsequently, impurities are doped to form the source and drain regions 410, 411. After that the insulating layer 414 is formed with contact holes as shown in Figure 8(c). Thermal diffusion or ion implantation techniques are generally used for doping impurity to form the source and drain regions. Then the data signal line 415 is formed as shown in Figure 8(d) and the driving electrode 416 is formed as shown in Figure 8(e). The signal line 415 cannot be formed at the same time as the driving electrode 416. The intrinsic polycrystalline silicon layer 409 in the channel region may have a thickness of less than 2500Å discussed above.

The unique characteristics of the active matrix

liquid crystal display device of Figures 7 and 8 is that an intrinsic polycrystalline silicon layer is used for the channel region and, by thermally oxidizing this intrinsic polycrystalline silicon layer, a gate insulating film is formed.

The reason why the intrinsic polycrystalline silicon layer is used for the channel region is so that the ON current is relatively large and simultaneously the OFF current is limited. The ON current is relatively large since polycrystalline silicon has a carrier mobility of about 10 $cm^2/Vsec$. In addition, OFF current can be minimized by using intrinsic polycrystalline silicon without any impurity and/or by reducing its thickness.

In a conventional MOS type transistor utilizing monocrystalline silicon, the PN junction (where the P-type substrate is used for the N-channel and the N-type substrate is used for the P-channel are in contact) is utilized to decrease OFF current. On the other hand, in the case of utilizing polycrystalline silicon, favourable formation of a PN junction cannot be attained and hence OFF current cannot be decreased sufficiently.

Figure 9 shows the relationship between the concentration of impurities diffused into a channel region of an N-channel thin film transistor and OFF current, the data being obtained by experiment. Boron is used as the impurity which is diffused by ion implantation so as to form a P-type channel region. The abscissa in Figure 9 represents the amount of diffused boron, and the ordinate represents the amount of OFF current in the case where the gate voltage is zero.

It will be appreciated from Figure 9 that OFF current is a minimum when no impurity is diffused in the channel region, namely, the channel region is intrinsic polycrystalline silicon. This is because leakage current at a PN junction increases as concentration of impurities increases. On the other hand, in the case of forming an N-type channel region, namely, a depletion-type transistor, OFF current increases. Accordingly, OFF current can be minimized when the channel region is intrinsic polycrystalline silicon.

Thermal oxidation of the intrinsic polycrystalline silicon to form the gate insulating film enables a relatively large ON current to be obtained, and a superior thin film transistor is provided for stability, reproducibility and reliability. To this end, the polycrystalline silicon needs to be thermally oxidized at a temperature higher than 900°C. Grain size of the crystalline particles becomes larger and their mobility greatly increases at this temperature. As well-known, in the case of forming a gate insulating film by thermal oxidation of a polycrystalline silicon layer the interfacial level between the polycrystalline silicon and its thermal oxidation film can be made smaller compared to the case where th gate insulating film is formed as a silicon dioxide film by, for example a sputtering technique or a vapour phase growth technique. Thus, th threshold voltage of the thin film transistor can be reduced. That is, a relatively large ON current flow can be attained by utilizing intrinsic polycrystalline silicon having a larg mobility and a low thresh ld voltag as the channel region.

Furthermore, a superior stability, reproducibility and reliability can be provided by thermally oxidizing this polycrystalline silicon layer to form the gate insulating film. That is, a superior interface usually having a smaller value of the interfacial level can be stably formed so that stability and reproducibility of the thin film transistor are greatly improved, and also reliability is markedly improved since the interface is formed utilizing stable materials such as silicon and a thermal oxidation film thereof by the same process as that used in ordinary silicon semiconductor technology.

As mentioned above thermal treatment of the polycrystalline silicon layer at a temperature higher than 900°C is required to form the gate insulating film. For this, an insulating substrate, for example, of quartz glass, which has a relatively high melting point must be used as the substrate. This raises manufacturing cost since high melting point substrates are more expensive than low-melting point substrates. To counteract this, it is necessary to reduce the cost of manufacturing a film thin transistor. Generally, a relatively complicated manufacturing process is needed to form a substrate of an active matrix liquid crystal display device. Thus it is desirable to simplify manufacture in order to reduce the costs. In view of this, it is desirable to form the data signal lines and driving electrodes from a single transparent conductive film.

Figure 10 illustrates another embodiment of an active matrix liquid crystal display device according to the present invention where a data signal line and a driving electrode are formed from the transparent conductive film. Fundamentally the construction is the same as shown in Figures 7 and 8 except for the data signal line 415 and the driving electrode 416. Indium oxide, tin oxide or indium-tin oxide is used for the transparent conductive film. Step 8(d) can be omitted by this construction. It is most effective to simplify the patterning process to reduce manufacturing costs, since the patterning process, usually a photo-etching process, accounts for a large percentage of manufacturing cost of any semiconductor device. Five patterning processes are required in the manufacturing process illustrated in Figure 8, however, four patterning processes are sufficient to form the liquid crystal display device shown in Figure 10. In addition, it is unnecessary to form two kinds of conductive films. Such a simplification of the manufacturing process is extremely effective to form an inexpensive active matrix liquid crystal display device.

CLAIMS

1. A thin film MOS transistor including a silicon layer whose thickness, at least in the channel region, is less than 2500Å.

2. A thin film MOS transistor as claimed in claim 1 in which the thickness of the silicon layer in the channel region is less than its thickness in the source and drain regions.

3. A thin film MOS transistor as claimed in claim 1 or 2 in which the silicon layer is a polycrystalline

silicon layer.

4. A thin film MOS transistor as claimed in any preceding claim in which the silicon layer is an intrinsic polycrystalline silicon layer.

5. A thin film MOS transistor substantially as herein described with reference to and as shown in Figure 5 or Figure 6 of the accompanying drawings.

6. An active matrix liquid crystal display device having a plurality of picture elements arranged in a matrix, each picture element having a thin film MOS transistor as claimed in any preceding claim as a switching element.

7. An active matrix liquid crystal display device having a plurality of data lines and address lines arranged in columns and rows, a thin film MOS transistor and a liquid crystal driving electrode being formed at the intersection of each data line with each address line, each thin film MOS transistor having a channel region of intrinsic polycrystalline silicon.

8. An active matrix liquid crystal display device as claimed in claim 7 including a gate insulating film formed by thermally oxidizing the intrinsic polycrystalline silicon.

9. An active matrix liquid crystal display device as claimed in claim 7 or 8 in which the data lines and the display electrodes are formed from the same transparent conductive film.

10. An active matrix liquid crystal display device substantially as herein described with reference to and as shown in Figure 8 or Figure 10 of the accompanying drawings.

11. A thin film MOS transistor composed of silicon thin film, characterized in that the thickness of said silicon thin film in the channel region is thinner than that in the source and drain regions.

12. A thin film MOS transistor composed of silicon thin film, characterized in that the thickness of said silicon thin film is less than 2500Å.

13. An active matrix assembly for liquid crystal display device including a plurality of data lines and address lines in the matrix arranged in column and rows, a plurality of thin film transistors and electrodes for driving liquid crystal are located at the cross point of said data line and address line, wherein the channel region of said thin film transistor is formed of intrinsic polycrystalline silicon, the gate insulating film by oxidising said intrinsic polycrystalline silicon film with thermal treatment.

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